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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/064,615	07/31/2002	Sheng-Hung Lin	9034-US-PA	6860

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JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
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EXAMINER	
CHEN, KOU YI	
ART UNIT	**PAPER NUMBER**
2193	

DATE MAILED: 02/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/064,615	LIN ET AL.	
	Examiner	Art Unit	
	Kou-Yi K. Chen	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *4 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6 and 18-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 18-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 July 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to the application filed on July 31, 2002.

2. Claims 7-17 and 24-28 have been cancelled by the applicants.

3. Claims 1-6, and 18-23 are pending in the application.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claim 1 recites the limitation "the write pin" in line 6. There is insufficient antecedent basis for this limitation in the claim. For examination purpose, this limitation is interpreted as "a write pin".

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-6 and 18-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,170,043 to Hu (hereinafter, "Hu") in view of US Patent 6,577,301 to Tsai et al. (hereinafter, "Tsai").

As per claim 1

Hu teaches:

a rewritable memory ("update firmware information, which is stored in a memory 210, such as a flash memory 210 or an electrical erasable programmable ROM (EEPROM)" in col. 3 lines 23-25, and "A conventional method to update the firmware usually puts all firmware data and the execution program for update in a single ROM" in col. 1 lines 40-45), containing a main control program with a writing function ("The update program includes a program code, and an update program routine" in col. 4 lines 13-14 , and "the program code is treated as data that is the firmware information to be updated" in col. 4 lines 25-26), wherein the main control program by the writing function can be erased from the rewritable memory and an upgrade main control program can be written into the rewritable memory via the write pin ("The original program code data stored in the flash memory 212 are compared with the program code data from the buffer memory 202, and are updated" in col. 4 lines 26-29, also, it is an inheritance that memory chips all equipped with pins for input and output purpose); and

a controller coupled to the rewritable memory ("a controller 208" in col. 3 line 27, also see FIG. 2, where the Controller 208 is coupled to the Flash Memory 210), comprising:

a built-in storage unit, temporarily storing an update subroutine ("the extra memory 202 is used to store the update program routine " in col. 4 lines 17-18) of the main control program by using a continuous mapping address ("the update program routine is downloaded into the extra memory 202, the microprocessor 204 will jump to a special address, such as the F880h of FIG. 3B, which is determined by the extra memory 202. The special address is used to update the program code of the flash memory 210" in col. 5 lines 3-7, also see FIG. 3B, where address F880h to address FFFFh is marked as Reserve, and it is a continuous address space), wherein the built-in storage unit comprises a control register for temporarily storing a control signal ("sends these signals to the external ROM" in col. 2 lines 10-11, the signals have to be stored before being recognized);

a microprocessor, built at outside or inside of the controller ("The microprocessor 204 is separately coupled to the extra memory 202, the decoder 206, the controller 208, and the flash memory 210" in col. 3 lines 31-34); and

a control interface, coupled to the rewritable memory, the built-in storage unit and the microprocessor ("FIG. 5 is a structure diagram of control signal, schematically illustrating a control relation between the microprocessor and the flash memory" in col. 4 lines 1-3), wherein the control interface receives the control signal temporarily stored in the control register of the built-in storage unit to determine a fetch priority of the built-in storage unit and the rewritable memory ("The microprocessor 204 produces an indicator

flag to a switch circuit 209 so as to switch the CD-ROM system to the update programming mode. The flash memory 210 is switched to a status serve as a memory space of the program code dada, and the microprocessor 204 also read instructions of an instruction stack, which is stored in the extra memory 202, from the highest-address. The data stored in the buffer memory 210 are access through the decoder 206" in col. 5 lines 7-14) and to build up a write channel between the microprocessor and the rewritable memory ("the microprocessor 204 produces control signals, such as a chip select (CS) signal, a writing-in (WR) signal, and an output enable (OE) signal, to control the flash memory 210" in col. 5 lines 15-18);

wherein the microprocessor reads out the update subroutine stored in the rewritable memory, writes the update subroutine into the continuous mapping address of the built-in storage unit by the control interface, and fetches and executes the update subroutine in the built-in storage unit to write the upgrade main control program into the rewritable memory ("The micro processor 204 reads instructions, which reside in the update program routine, from the extra memory 202 and executes the instructions. The program code data stored in the buffer memory 212 are sequentially written into the flash memory 210, which serves as a memory space for the program code data. Here, the program code is treated as data that is the firmware information to be updated" in col. 4 lines 20-26).

Hu does not explicitly teach the firmware update system is applied in a liquid crystal panel display controller. However, Tsai discloses in an analogous system that in a more advanced monitor system, a read only memory including an erasable programmable read only memory is built in, so that by refreshing the read only memory, the modification of functions, software debugging or font alteration can be achieved (see Tsai col. 1 lines 24-29).

It would have been obvious to a person of ordinary skill in the art at the time of the invention was made to modify the teachings of Hu with the advanced controller system as taught by Tsai.

The modification would have been obvious because one of the ordinary skill in the art would have been motivated to refresh the controller software without having to physically adjust the jumpers on the hardware (see Tsai col. 2 lines 11-14) in Hu's disclosed system, using Tsai's suggestion in col. 1 lines 24-29.

As per claim 2, the rejection of claim 1 is incorporated, and further, Hu teaches: the type of the rewritable memory comprises a flash-ROM or an EEPROM ("update firmware information, which is stored in a memory 210, such as a flash memory 210 or an electrical erasable programmable ROM (EEPROM)" in col. 3 lines 23-25).

As per claim 3, the rejection of claim 1 is incorporated, and further, Hu teaches: the main control program and the update subroutine have a function call relationship ("The micro processor 204 reads instructions, which reside in the update program

routine, from the extra memory 202 and executes the instructions. The program code data stored in the buffer memory 212 are sequentially written into the flash memory 210, which serves as a memory space for the program code data. Here, the program code is treated as data that is the firmware information to be updated" in col. 4 lines 20-26, wherein the update program routine is called to copy the program code, which is the updated firmware, into flash memory).

As per claim 4, the rejection of claim 1 is incorporated, and further, Hu teaches: the storage address of the rewritable memory used to store the update subroutine is different from the storage address of the built-in storage unit used to store the update subroutine ("The micro processor 204 reads instructions, which reside in the update program routine, from the extra memory 202 and executes the instructions. The program code data stored in the buffer memory 212 are sequentially written into the flash memory 210" in col. 4 lines 21-24, note, if the update subroutine is stored at different storage locations, the physical address of the different storage locations can not be the same).

As per claim 5, the rejection of claim 1 is incorporated, and further, Hu teaches: if a fetch address sent by the microprocessor is equal to the continuous mapping address, the fetch priority belongs to the built-in storage unit ("The microprocessor 204 produces an indicator flag to a switch circuit 209 so as to switch the CD-ROM system to the update programming mode. The flash memory 210 is switched to a status serve as

a memory space of the program code dada, and the microprocessor 204 also read instructions of an instruction stack, which is stored in the extra memory 202" in col. 5 lines 7-12).

As per claim 6, the rejection of claim 1 is incorporated, and further, Hu teaches:
if a fetch address sent by the microprocessor is not equal to the continuous mapping address, the fetch priority belongs to the rewritable memory ("The data stored in the buffer memory 210 are access through the decoder 206. The switch circuit 209 controlled by the microprocessor 204 produces control signals, such as a chip select (CS) signal, a writing-in (WR) signal, and an output enable (OE) signal, to control the flash memory 210" in col. 5 lines 13-18).

As per claim 18

Hu teaches:
An online firmware update method, applied in the liquid crystal panel display (see claim 1 rejection), wherein the liquid crystal panel display comprises a controller, which can be implemented internal or external of a microprocessor, and a rewritable memory, the online firmware update method comprises the steps of:

copying an update subroutine of the rewritable memory into a built-in storage unit of the controller ("At this update mode, the extra memory 202 is used to store the update program routine" in col. 4 lines 16-18);

enabling a control signal of the controller ("the microprocessor 204 produces control signals, such as a chip select (CS) signal, a writing-in (WR) signal, and an output enable (OE) signal, to control the flash memory 210" in col. 5 lines 15-18);

calling the update subroutine of the built-in storage unit by using a function call ("The micro processor 204 reads instructions, which reside in the update program routine, from the extra memory 202 and executes the instructions" in col. 4 lines 20-22);

erasing the rewritable memory ("The program code data stored in the buffer memory 212 are sequentially written into the flash memory 210" in col. 4 lines 22-24, therefore, the original contents in the flash memory are erased);

downloading an upgrade main control program ("the update firmware information has been downloaded in the computer 216 through the main board interface 214" col. 5 lines 41-43); and

writing the upgrade main control program into the rewritable memory to accomplish the online firmware update operation of the rewritable memory ("The micro processor 204 reads instructions, which reside in the update program routine, from the extra memory 202 and executes the instructions. The program code data stored in the buffer memory 212 are sequentially written into the flash memory 210" in col. 4 lines 21-24).

As per claim 19, the rejection of claim 18 is incorporated, and further, Hu teaches: the rewritable memory comprises a main control program, the main control program comprises the update subroutine ("The update program includes a program code, and an update program routine" in col. 4 lines 13-14 , and "the program code is treated as data that is the firmware information to be updated" in col. 4 lines 25-26), moreover the main control program and the update subroutine have a function call relationship ("The micro processor 204 reads instructions, which reside in the update program routine, from the extra memory 202 and executes the instructions. The program code data stored in the buffer memory 212 are sequentially written into the flash memory 210, which serves as a memory space for the program code data. Here, the program code is treated as data that is the firmware information to be updated" in col. 4 lines 20-26, wherein the update program routine is called to copy the program code, which is the updated firmware, into flash memory).

As per claim 20, the rejection of claim 19 is incorporated, and further, Hu teaches: the step of erasing the rewritable memory erases the main control program in the rewritable memory ("The micro processor 204 reads instructions, which reside in the update program routine, from the extra memory 202 and executes the instructions. The program code data stored in the buffer memory 212 are sequentially written into the flash memory 210, which serves as a memory space for the program code data. Here,

the program code is treated as data that is the firmware information to be updated" in col. 4 lines 20-26).

As per claim 21, the rejection of claim 18 is incorporated, and further, Hu teaches: the step of enabling the control signal builds up a write channel between the controller and the rewritable memory ("the microprocessor 204 produces control signals, such as a chip select (CS) signal, a writing-in (WR) signal, and an output enable (OE) signal, to control the flash memory 210" in col. 5 lines 15-18).

As per claim 22, the rejection of claim 18 is incorporated, and further, Hu teaches: the storage address of the rewritable memory used to store the update subroutine is different from the storage address of the built-in storage unit used to store the update subroutine ("The micro processor 204 reads instructions, which reside in the update program routine, from the extra memory 202 and executes the instructions. The program code data stored in the buffer memory 212 are sequentially written into the flash memory 210" in col. 4 lines 21-24, note, if the update subroutine is stored at different storage locations, the physical address of the different storage locations can not be the same).

As per claim 23, the rejection of claim 18 is incorporated, and further, Hu teaches:

the type of the rewritable memory comprises a flash-ROM or an EEPROM ("update firmware information, which is stored in a memory 210, such as a flash memory 210 or an electrical erasable programmable ROM (EEPROM)" in col. 3 lines 23-25).

Conclusion

8. The prior art made of record, and not relied upon, is considered pertinent to applicant's disclosure.

Contact Information

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Kou-Yi K. Chen** whose telephone number is **571-272-8592**. The examiner can normally be reached **from 8:30 am to 5:00 pm on M-F**.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kakali Chaki can be reached on 571-272-3719. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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